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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,365	04/07/2004	Xiaojun Wang	SILI 2828 (CAD: 03-114)	7698

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,365	WANG ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8,9,23 and 24* is/are allowed.

6)☒ Claim(s) *1-7,10-22 and 25-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/820,365 filed 04/07/2004 and amendment filed 09/05/2006.

2. Claims 1-30 remain pending in the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-7, 10-22, 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lampaert et al. (US Patent 6,588,002).

With respect to claim 1 Lampaert et al. teaches an integrated circuit (IC) physical verification method within LVS (layout versus circuit schematic) verification of the generated circuit layout (col. 2, ll.14-15) comprising the steps of: a. processing layout data describing positions of conductive material residing on layers of an IC including a drawn inductor having a spiral to produce recognition layer data representing a two-dimensional boundary shape of the spiral that is a composite of two-dimensional shapes of all conductive material forming the spiral (within integrated circuit design including a step of generating circuit layout data (col. 1, ll.22-24), wherein layout data includes

description of the integrated circuit design including spiral inductor shown on the schematic diagram of the Fig. 2 (col. 4, ll.18-21) and the spiral inductor resides on layers of the integrated circuit, i.e. on the metal (conductive) level 2 and metal level 1(col. 9, ll.29-33) and presented by Fig. 4 demonstrating a two-dimensional boundary shape of the spiral inductor (col. 8, ll.65-66), wherein spiral inductor 424 includes spiral inductor metal segments 426, which form an exemplary shape of square (col. 9, ll.10-12)); and b. processing the recognition layer data to generate parameter data describing a shape of the spiral the shape being divided into a plurality of polygonal segments for separate processing relating thereto (within determining a spiral inductor parameters, such as X_{size} 418 and Y_{size} 422, number of turns 406, spacing 410, width 414 as shown on the Fig. 4 (col. 9, ll.1-3), wherein as shown o the Fig. 4 spiral inductor 424 includes spiral inductor metal segments 426, which form an a shape of layout (col. 9, ll.10-12)).

With respect of claim 16 Lampaert et al. teaches computer-readable media containing software which when read and executed by a computer causes the computer to carry out an integrated circuit (IC) physical verification method (within a computer system shown on the Fig. 7, which can be utilized to implement a design of the integrated circuit including step of verification of the design IC inducing a data of a layout of a spiral indictor as shown on the Fig. 6 (step 610) (col. 12, ll.36-40; col. 11, ll.44-46)), comprising the steps of: a. processing layout data describing positions of conductive material residing on layers of an IC including a drawn inductor having a spiral to produce recognition layer data representing a two-dimensional boundary shape of the spiral that is a composite of two-dimensional shapes of all conductive material

forming the spiral (within integrated circuit design including a step of generating circuit layout data (col. 1, ll.22-24), wherein layout data includes description of the integrated circuit design including spiral inductor shown on the schematic diagram of the Fig. 2 (col. 4, ll.18-21) and the spiral inductor resides on layers of the integrated circuit, i.e. on the metal (conductive) level 2 and metal level 1(col. 9, ll.29-33) and presented by Fig. 4 demonstrating a two-dimensional boundary shape of the spiral inductor (col. 8, ll.65-66), wherein spiral inductor 424 includes spiral inductor metal segments 426, which form an exemplary shape of square (col. 9, ll.10-12)); and b. processing the recognition layer data to generate parameter data describing a shape of the spiral the shape being divided into a plurality of polygonal segments for separate processing relating thereto (within determining a spiral inductor parameters, such as X_{size} 418 and Y_{size} 422, number of turns 406, spacing 410, width 414 as shown on the Fig. 4 (col. 9, ll.1-3), wherein as shown o the Fig. 4 spiral inductor 424 includes spiral inductor metal segments 426, which form an a shape of layout (col. 9, ll.10-12)).

With respect to claims 2-7, 10-15, 17-22, 25-30 Lampaert et al. teaches:

Claims 2, 17: further comprising the step of: c. processing the recognition layer data to determine whether the spiral has turns of uniform width by indicating all segments of spiral inductor layout and their width and confirming that all segments have equal width (uniform) as demonstrated by a table of the Fig. 3 (col. 6, ll.15-19);

Claims 3, 18: further comprising the step of: c. processing the recognition layer data to determine whether all bends in the spiral are of uniform bend angle within determination of the shape of the spiral inductor layout, which might be a square as

demonstrated by the Fig. 4, wherein each angle of bending the segment of the spiral inductor equal to 90° (col. 9, ll.10-12);

Claims 4, 19: further comprising the step of: d. processing the recognition layer data to identify a position of the spiral within determining spiral inductor parameters such as Y_{size} and X_{size} to indicate a total width of spiral inductor in the x direction and y direction, which might be used for determination a position of the spiral inductor in the integrated circuit layout (col. 4, ll.61-64);

Claims 5, 20: wherein the parameter data indicates at least one of the following: a length of the spiral, a width of conductive material forming turns of the spiral, and spacing between conductive material turns of the forming the spiral within determining parameters of the spiral inductor shown on the Fig. 4, wherein such parameters as X_{size} (length of spiral), Y_{size} (width if spiral), spacing 410 as spacing between adjacent metal segments (col. 9, ll.1-3);

Claims 6, 21: wherein the parameter data indicates at least one of the following: a number of sides of the spiral, and a diameter of an area bounded by the spiral within determining parameters of the spiral inductor shown on the Fig. 4, wherein number of turns 406 determines number of sides of the spiral, wherein a distance between first and last metal segments might be calculated as diameter of an area bounded by the spiral (col. 9, ll.41-47);

Claims 7, 22: further comprising the step of: c. processing the recognition layer data to determine whether all bends in conductors forming the spiral are of uniform bend angle by determination the shape of the spiral of the inductor, such as a square as

shown on the Fig. 4, wherein square has all right (90°) angles as uniform (col. 9, ll.10-12);

Claims 10, 25: wherein the boundary shape includes a plurality of polygonal shapes representing shapes of conductive material forming the spiral within presenting the inductor in a variety of configurations and shapes, such as spiral, non-spiral inductors, having the shape of square, rectangular, octagonal spiral inductors (col. 13, ll.20-31), and wherein step b comprises the substeps of: b1. processing the recognition layer data to identify each polygonal shape and to determine a length of each identified polygonal shape as shown on the Fig. 5, wherein rectangular shape of the spiral inductor is represented as layout 524 including X_{size} 518 (length of the rectangular/shape)Y_{size} 522 (width of the shape/rectangular), and b2. summing the computed lengths of the polygonal shapes to determine a length of the spiral within other parameters characterizing the shape of spiral inductor including number of turns 506, width 514, spacing 510 for calculating the length of the spiral (col. 10, ll.1-6).

Claims 11, 26: wherein the boundary shape includes a plurality of polygonal shapes representing shapes of conductive material forming the spiral within presenting the inductor in a variety of configurations and shapes, such as spiral, non-spiral inductors, having the shape of square, rectangular, octagonal spiral inductors (col. 13, ll.20-31), and wherein step b comprises the substep of: b1. processing the recognition layer data to identify each polygonal shape and to determine a width of each identified polygonal shape within determination of each metal segment 426 and their shape (col. 9, ll.30-33) shown on the Fig. 4 including width 414 and number of turns 406;

Claims 12, 27: further comprising the step of c. processing the recognition layer data boundary shape to generate a netlist representation of the drawn inductor as shown on the Fig. 2, which is a schematic diagram of an spiral inductor subcircuit model represents a netlist of the spiral inductor (col. 4, ll.28-41);

Claims 13, 28: wherein the netlist representation of the drawn inductor includes data describing physical characteristics of the inductor influencing its inductance within a table 300 shown on the Fig. 3 containing parameters from the schematic diagram on the Fig. 2 and calculating inductance of the spiral inductor (col. 8, ll.33-40);

Claims 14, 29: further comprising the steps of: c. processing the recognition layer data to determine a position of the inductor within the layout based on a position of the boundary shape of its spiral indicated by the recognition layer data within determining spiral inductor parameters such as Y_{size} and X_{size} to indicate a total width of spiral inductor in the x direction and y direction, which might be used for determination a position of the spiral inductor in the integrated circuit layout (col. 4, ll.61-64); d. processing the recognition layer data to determine whether all bends in conductors forming the spiral are of uniform bend angle within determination of the shape of the spiral inductor layout, which might be a square as demonstrated by the Fig. 4, wherein each angle of bending the segment of the spiral inductor equal to 90° (col. 9, ll.10-12); e. processing the layout data to determine whether conductive material residing on separate layers and forming portions of the spiral inductor are interconnected within determination in the layout of metal segments 426 of the spiral inductor and their terminals 428 and 430 having connection in the different metal levels (col. 9, ll.29-33);.

Claims 15, 30: further comprising the steps of f. processing the recognition layer data to determine parameters relating to a shape of the spiral influencing the spiral's inductance within a table 300 shown on the Fig. 3 containing parameters from the schematic diagram on the Fig. 2 and calculating inductance of the spiral inductor (col. 8, ll.33-40); and g. processing the data representing the layout to generate a netlist description of the spiral inductor including the parameters determined at step f within step 610 of the Fig. 6 showing the verification of the circuit layout within LVS to generate final layout representing the same topology specified by the circuit schematic (col. 11, ll.45-57).

Allowable Subject Matter

6. Claims 8, 9, 23 and 24 are allowed. The prior art of record does not teach or suggest a combination of steps/elements in claim 8 and similarly recited claims 9, 23 and 24 among other steps/elements wherein the second binary data distinguishes positions of all conductive material forming the spiral from positions of any conductive material forming the center tap/spoke/terminal (claims 8 and 9); and wherein the second binary data indicates positions of all conductive material forming the spiral and refrains from indicating positions of any conductive material forming the center tap for determining an area of overlap between the center tap and spiral (claim 23 and 24).

Remarks

7. In remarks Applicant argues in substance:

a) "the reference nowhere either discloses or suggests a verification method wherein recognition layer data is processed in such manner that the spiral shape of the

given conductive material is "divided into a plurality of polygonal segments", as claims 1 and 16 now clarify much less "for separate processing relating thereto"".

8. Examiner respectfully disagrees for the following reasons:

As to a) It has to be noted that "verification method" is mentioned only in the preamble of the claim 1, and does not give any weight to the invention, because no steps of the verification of the circuit design are described in the body/limitations of the claim. Therefore the argument that the reference (Lampaert et al.) nowhere either discloses or suggests a verification method is irrelevant. However Lampaert et al. teaches circuit design as shown on the Fig. 6 (col. 10, ll.10-13) including step of verification of the circuit layout generated in step 608 (col. 11, ll.45-47). Moreover, as shown o the Fig. 4 spiral inductor 424 is divided into a plurality of polygonal metal segments 426, which form an a **shape of layout** (c33ol. 9, ll.10-12)), wherein data for each metal segment is processed separately (col. 10, ll.48-52).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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